Notice of Allowability	Application No.	Applicant(s)
	10/613,006	KELLAR ET AL.
	Examiner	Art Unit
	Jennifer M. Dolan	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdt of 10/28/05*.

2. ☒ The allowed claim(s) is/are *1-3, 5, 6, 8-10, 12, 13, 15-18, 20, 22-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 11/4/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Drawings

1. The replacement drawing sheet for figure 3 was received on 10/28/05. The replacement drawing is approved.

Allowable Subject Matter

2. Claims 1-3, 5, 6, 8-10, 12, 13, 15-18, 20, and 22-25 are allowed.

3. The claims are considered allowable for the reasons deemed to be of record, as listed in the 4/12/05 Office Action, as well as the Applicant's remarks of 5/26/05 and 10/28/05, and additionally for the following reasons:

Regarding claims 1-3, 5, 6, 8-10 12, 13, 15-18, 20, 22, and 23, the claims specifically require the presence of active IC components on each of the adjacent, bonded wafers. It is noted that many of the cited prior art references are of MEMS type devices with a hermetically sealed cavity, such devices including a top substrate having only passive interconnections or circuitry components and no active ICs (see, for example, US 6,643,920 to Hori, US 6,297,072 to Tilmans et al., and US 6,373,130 to Salaville). Since there is generally no motivation in the art for applying a MEMS-type hermetic seal to a non-MEMS wafer stack, nor is there motivation for supplying active ICs to a MEMS cover substrate, it is the Examiner's opinion that the prior art MEMS references are not particularly applicable to the claimed invention of claims 1-3, 5, 6, 8-10, 12, 13, 15-18, 20, 22, and 23.

Regarding claims 1-3, 5, 6, 9, 10, 12, 13, and 24, the primary reason for allowance is that the claims require a barrier layer disposed on the outer periphery of each of two wafers, each wafer including a plurality of dice, where the barrier layers are bonded to form a sealed wafer stack, and where the barriers protect the dice from corrosion, contamination, and crack propagation when the wafers are singulated. The most relevant prior art of record includes US 6,724,084 to Hikita, US 5,699,611 to Kurogi, and US 5,455,445 to Kurtz, which teach depositing a barrier layer at the outer periphery of a single IC die, and then bonding the die to a second substrate, such that the barrier layer seals the die/substrate structure. These references, however, provide no suggestion of applying barrier layers to the periphery of an entire wafer that will subsequently be singulated, and in the Examiner's opinion, teach away from providing a barrier layer around the entire wafer, since such a structure would not provide the individually hermetically sealed dice after singulation, as disclosed by the prior art references.

Regarding claims 8, 15-18, 20, 22, and 25, the primary reason for allowance is that the prior art fails to suggest barrier structures applied to the periphery of two dice such that the barrier structures are joined when the dice are bonded, where the barrier structures are in the form of concentric rings or a dense grid of copper lines, as required by the claims. Instead, the prior art of record, including even the hermetic MEMS structures, only use a single ring barrier structure at the periphery of the dice, and provide no teaching or suggestion of structures other than a single ring barrier. Since the concentric ring structure and the dense grid structure provide unexpected improvements in mechanical strength near the saw lines as well as improved resistance to oxygen permeability through the barrier structure based on oxidation of the outer or

single ring, it is the Examiner's opinion that the claimed features would not have been obvious to a person having ordinary skill in the art.

Regarding claim 23, the primary reason for allowance is that the claim requires that two stacked IC wafers or dice be bonded and have a peripheral barrier structure before device thinning (such that the barrier structure is capable of protecting the metallic lines during the thinning process). Since the prior art of record dealing with die or wafer edge barrier structures no not teach or suggest wafer thinning at all, and since wafer thinning, if it is to be applied at all to the wafer, is generally applied to a non-singulated wafer, as opposed to an individual die, it is the Examiner's opinion that a person skilled in the art would not have found any motivation for performing a wafer thinning step to a die after singulating the die from the wafer, bonding the die to a second die, and applying a barrier structure. Alternatively, claim 23 could be interpreted as requiring a step of placing barrier layers on the peripheries of two bonded wafers, the wafers including multiple dice, a wafer thinning step, and then a singulation step. This situation, however, is substantially similar to that of claims 1-3, 5, 6, 9, 12, 13, and 24, and is allowable for the reasons listed above in the treatment of those claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

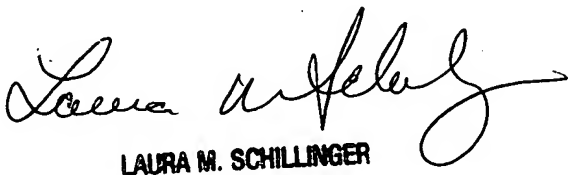
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd



LAURA M. SCHILLINGER
PRIMARY EXAMINER